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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,294	12/15/2000	Santo Maggio	Q62156	8429

7590 02/27/2004

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EXAMINER	
VARTANIAN, HARRY	

ART UNIT	PAPER NUMBER
2634	6

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/736,294	MAGGIO ET AL.	
	Examiner	Art Unit	
	Harry Vartanian	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,11,13,14 and 16* is/are rejected.

7)☒ Claim(s) *7,9,10,12,15,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Objections

1. Claim 11 is objected to as being an indefinite multi-dependent Claim. It is uncertain if the Claim is dependent on just Claim 1 or additional Claims because of the phrase "to any of Claims 1."

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claim 1, 13, 14, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ozkan(US Patent# 5488641). Regarding Claim 1, Ozkan meets the following limitations:

> A method for recovering a clock signal from an input data signal **(abstract)** in a telecommunications system, the method comprising the steps of-
>
> comparing the input data signal with a recovered clock signal in order to control said recovered clock signal generation; and **(Column 2, Lines 38-43)**
>
> generating a plurality of delayed clock signals, obtained by multi-delaying at least a reference signal, said delayed clock signals being phase-shifted with respect to each other, **(Column 2, Lines 52-66)**
>
> wherein said delayed clock signals show a phase shift with respect to each other, that is nominally constant in time, and **(Column 1, Line 63 to Column 2, Line 6)**
>
> wherein it further comprises the step of selecting the recovered clock signal among said delayed clock signals. **(Column 3, Lines 57 to Column 4, Line 15)**

Regarding Claim 13, Ozkan meets the following limitations:

> Circuit for recovering a clock signal from an input data signal **(abstract)** in a telecommunications network,
>
> the circuit comprising a phase comparator comparing the input data signal phase and the recovery clock signal phase for supplying a phase information, **(fig 3 items 370 and 340)**
>
> which controls generating means of said recovery clock signal, **(Column 3, Lines 57 to Column 4, Line 15)**
>
> wherein said generating means comprise a delay line having a plurality of taps for generating a plurality of delayed signals. **Fig 3**

Regarding Claim 14, Ozkan meets the following limitations:

> wherein said generating means comprise selection means of the recovered clock signal. **(Column 3, Lines 57 to Column 4, Line 15)**

Regarding Claim 16, Ozkan meets the following limitations:

> wherein said selection means comprise, moreover, a control logics driving the first selection block and the second switch block according to the phase information supplied by the phase comparator. **Fig 5**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 2-6, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozkan(US Patent# 5488641) in view of Gersbach et al(US Patent # 5,371,766). Ozkan meets all the limitations of Claim 2 except for the disclosure of "the sum of the shifts associated to such delayed signals covers the bit period of the input data signal".

However, Gersbach et al discloses:

> "The **sum of the delays of the n phase-delayed signals corresponds to the period T_{local} of the local clock signal 52**. The period T_{local} equals 125 nanoseconds for the 4 Mbits/sec rate or 31.25 nanoseconds for the 16 Mbits/sec rate. Each of these phase-delayed signals is shifted in time about 1/n of a local clock signal period. For example, for a local clock signal period T_{local} and a resolution of 10%, ten phase-shifted signals are output by the delay element, each of the signals being shifted successively in

> time by $T_{local}/10$. Of course, more or less than ten phase-shifted signals may be implemented. Generally, the greater the number of phase-delayed signals output by the delay element, the greater the phase resolution. As an alternative to a delay element, a series of n gates could be used, each having an inherent propagation delay of T_{local}/n." **(Column 5, lines 37-54)**

Therefor it would have been prima facie obvious to those skilled in the art at the time the invention was made to have a taped delay line of shifted delayed clock signals where the sum of the shifts equaled one bit or clock period. The motivation to combine is that for fine phase detection the phase shift typically used is less than the clock period in order to ensure that the shift does not overshift and miss the trigger edges of the clock signal.

Regarding Claim 3, Gersbach et al meets the following limitations:

> wherein it further comprises the step of dynamically changing the number of delayed signals by comparing the bit period with the shift sum. **(Column 5, lines 37-54)**

Regarding Claim 4, Gersbach et al meets the following limitations:

> wherein the shift between each adjacent pair of delayed signals is nominally equal. **(Column 5, lines 37-54)**

Regarding Claim 5, Gersbach et al meets the following limitations:

> wherein it comprises the step of obtaining said plurality of delayed clock signals by multi-delaying a single sole reference signal. **(Column 5, lines 37-54)**

Regarding Claim 6, Gersbach et al meets the following limitations:

> wherein it further comprises the step of selecting a first recovery signal and a second recovery signal before selecting the recovery clock signal. **Claim 9**

Regarding Claim 8, Gersbach et al meets the following limitations:

> wherein it comprises the step of shifting the first recovery signal and the second recovery signal by one time interval. **(Claim 9 and Column 5, lines 37-54)**

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozkan(US Patent# 5488641) in view of Gersbach et al(US Patent # 5,371,766). Ozkan meets all the limitations of Claim 11 except for "to obtain a plurality of samples for each sampling cycle".

However, Gersbach et al discloses:

> "The series of histogram counters 36 comprises counters 36a through 36n, one counter for each time interval established by the data edge sorting circuit 34. Each of the individual counters 36a-36n counts the number of positive and negative going transitions occurring during its respective time interval and stores this information by conventional means. Thus, the particular counts 58a-n associated with each of the n equal time intervals into which T_{local} is divided provide a real time history of transitions in the received data signal, enabling development of a continuous histogram of the transition phase distribution with respect to the local clock signal. **By determining in real time the phase of the data signal with respect to the local clock signal, the optimal sampling points of the data signal may be ascertained. These optimal sampling points vary over real time, and thus the system provides a determination of the optimal sampling points based on changing operating conditions.**" **(Column 6, lines 29-47)**

Therefor it would have been prima facie obvious to obtain a plurality of samples for each sampling cycle. The motivation to combine is disclosed by Gersbach where he states that sampling over the period of a cycle provides the system a way of determining optimal sampling points.

Allowable Subject Matter

4. Claims 7, 9, 10, 12, 15, 17, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please consider these documents in their entirety:

US5901190

US6636979

US5712884

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Vartanian whose telephone number is 703.305.8698. The examiner can normally be reached on 9-5:30 Mondays to Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703.305.4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Harry Vartanian
Examiner
Art Unit 2634

HV

STEPHEN CHIN
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